REMARKS

This amendment is in response to the Final Office Action of 12/28/2009. The responses and section headings are in the same order as issues are set forth in the Office Action.

Claims 10, 15, and 21 are re written in independent form, as set forth in the Office Action, and are now in condition for allowance.

Claims 1-9, 11-14, 20, and 22-30 are still in this application and are believed to be patentable over the art of record, for reasons set forth herein.

A. Specification

The Examiner objects to the amended Abstract and suggests that "re-sequence" (page 14, line 3) should be changed to –re-sequenced- and "process" (page 14, next to last line) should be changed to –processed- . An amended Abstract complying with the Examiner's suggestions is submitted herewith.

B. Claim Objections

The Examiner objects to Claims 1-9, 11, 13-17, 19, 20, 22, 23, 28, and 29. The reasons for the objections and recommendations to correct them are set forth on pages 2-4 of the Office Action. For brevity, the reasons and recommendations for correction are not repeated in this document. However, except for the objection that Claim 16, line 2, "the data products "lacks antecedent basis, the referenced claims are amended to correct each of the objections. With respect to Claim 16, line 2, there is no recitation of "the data products". Instead, Claim 16, line 2, recites "the data packets" and it is amended by deleting –the-.

In reviewing the application, a typo is detected in Claim 30, line 3. In particular, "panes" should have been –planes- and the Claim is amended by changing "panes" to –planes-.

C. Claim Rejections - 35USC 103

Claims 1, 11, 13, and 16 – 21 are rejected under 35USC 103 (a) as being unpatentable over Salamat (US 20030012200A1) in view of Sasagawa (US20080253379A1).

With respect to Claim 1 applicants contend the references single or in combination do not teach the first three elements, of the Claim, namely:

a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows;

means for allocating a temporary storage location in a packet buffer to each received data packets;

means using predefined parameters for pointing to an output register previously assigned to receive data packets from a corresponding flow;

Because the references single and /or in combination do not teach or suggest these limitations, a Prima Facie case of obviousness has not been established and applicants are not obligated to provide further argument to traverse the rejection. As a consequence, Claim 1 and dependent Claims 11-13 are not obvious in view of the cited references.

To establish a prima facie case of obviousness three basic criteria must be met. MPEP 2142. First there must be a suggestion or motivation to modify or combine the references. In re Vaeck, 947 F 2d 488, 493; 20 USPQ 1438, 1442 (Fed.Cir.1991). Second, there must be a reasonable expectation of success in the modification or combination. In re Merck & Co., Inc.. 800 F. 2d 1091, 1097; 231 USPQ 375,379 (Fed. Cir. 1986). Finally, the

modification or combination must teach or suggest all of Applicants claimed limitations. In re Royka, 490 F.2d 981, 985; 180 USPQ 580, 583 (CCPA 1974).

Applicants are not obligated to present rebuttal evidence or arguments traversing the obviousness rejections until a Prima Facie case of obviousness have been established. As will be argued hereinafter a Prima Facie case of obviousness has not been made relative to any of the rejected claims. As a consequence, Claims 1-30 are patentable over the art of record.

In attempting to establish obviousness, the Examiner, at page 5 of the Office Action, maps Salamat to Claim 1 or visa versa and seems to suggest that paragraph [0010] of Salamat teaches "a plurality of flows", recited in the first element of Claim 1.

Applicants respectfully traverse this construction of Salamat on the grounds that paragraph [0010] does not teach or suggest "a plurality of flows". Instead, a review of Salamat paragraph [0010] refers to a reduced storage in which sequence numbers of packets are stored. There is no reference to flow. Therefore, reliance on this paragraph for teaching and/or suggesting "flows" is misplaced.

The Examiner seems to rely on the memory space 94 set forth in Salamat paragraph [0028] for teaching "a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows" recited in applicants Claim1.

It is applicants' contention that this construction of Salamat is in error. Paragraph [0028] states, in part, "The resequencing engine further includes sequence space in the form of memory 94 which is allocated for storing sequence numbers of data packets received by the egress board 40" This is a clear and unequivocal teaching of the function for memory 94 of Salamat and the attempt of the Examiner to map this to suggest the plurality of registers in Claim 1 would be anti thetical to the teachings of Salamat. In fact, the Examiner's construction of this feature of Salamat would destroy the purpose

of the reference and is further evidence of the failure to establish a Prima Facie case of obviousness.

The second element of applicants Claim 1 calls for "means for allocating a temporary storage location in a packet buffer to each receive data packet". The Examiner has not identified what part of the reference he is relying on to teach this element of applicants claim. Based upon long standing Patent Office practice and case law, the Examiner is obligated to do so. As argued above and incorporated herein by reference Salamat only teach a memory 94 for a specific purpose. It is applicants' contention that the memory cannot be used for disclosing both the plurality of registers and the packet buffer as recited in Claim 1. To use a single item in the reference to suggest two elements of applicants' Claim 1 would be improper.

In order to advance the prosecution of this application, applicants proffer amending Claim 1 as set forth above. In particular, this element of the claim 1 is amended as follows:

a packet buffer;

means for allocating a temporary storage location in said packet buffer to each received data packet.

This breakout of the element into its component parts would make it clearer that Claim1 disclose patentable subject matter over the art of record. Even if the Examiner refuses to enter this breakout version of this element, it is applicants contention that the non break out version of the element together with the other two elements mentioned above disclose patentable subject matter over the art of record.

Furthermore, applicants contend the Sasagawa reference does not disclose the limitations set forth above. In fact, the Examiner states that this reference is cited for teaching ingress adapter that is not taught in Salamat. This admission is further evidence that the limitations set forth above are not disclose in Sasagawa.

Claims 11 and 13 depend on Claim 1 and inherit the limitations discussed above by reason of their dependency. As a consequence, Claims 11 and 13 are patentable over the art of record.

Rejection of Claims 16- 20.

With due respect, applicants find the mapping of Claim 16 to Salamat or visa versa (page 6-9 Office Action) some what confusing. The Examiner's summaries or statements on Salamat may be correct but no reasonable construction of Salamat could suggest Claim 16 to an artisan. Apparently there appears to be a disconnection between the claimed elements and teachings in Salamat that the Examiner seems to rely on to teach or suggest the claimed elements.

For Example, Claim 16, in part, recites: " using the predefined parameters to search a memory and identifying a cross reference index; using the cross reference index associated with each received data packet to point to a respective output register previously assigned to the corresponding flow of each received data packet;" In mapping these elements of Claim 16, the Examiner (at page 8 of final Office Action) identifies paragraph [0053]. Applicants' construe this to mean the Examiner is relying on this paragraph to teach or suggest at least all or part of the claimed elements. A review of paragraph [0053] indicates that this paragraph only made general statements regarding expanding the invention and does not suggest anything that could be reasonable construed to suggest the claimed elements to an artisan. As a consequence, applicants contend the limitations set forth above is not found in Salamat. Therefore Claim 16 and dependent Claims 17-20 are patentable over the art of record. In an attempt to promote the prosecution of this application, it is suggested that Claim 16 be further limited by adding the following limitation:

"providing a plurality of registers with each register dynamically assigned to store received data packets from one of a plurality of flows. As is shown above, Claim 16 has been amended with this limitation".

Rejection of Claims 2-9, 11 and 22-23

Claims 2-9, 11, 22 and 23 are rejected under 35 U. S. C. 103(a) as being unpatentable over Salamat, in view of Sasagawa as applied to Claim 1 and 16 above, and further in view of Bryers (US20030126235A1)

Claims 2-9, 11, and 23 depend on Claim1 and inherit the limitations set forth above relative to Claim1. Neither of the secondary references Sasagawa nor Bryers suggests all three limitations identified above relative to Claim 1.Therfore, the arguments set forth above relative to Claim 1 is equally applicable to support the patentability of Claims 2-9, 11, and 23 and are incorporated herein by reference. As a consequence the Examiner has not established a prima facie case of obviousness, relative to these claims, and these claims are patentable over the art of record.

Claim 2 is patentable distinct in that it recites the details of the means for pointing to an output register. These details are not found in any of the references singly and/or in combination. The Examiner relied on Bryers for teaching the subject matter set forth in the Claim. It is Applicants' contention that among other things Bryers does not suggest—an associated identifier field including a cross reference index to point to a previously assigned output register among a plurality of output register. The Examiner, at page 11 of the Final Office Action, maps Claim2 to Bryers or visa versa but fails to identify where in Bryer this feature of Claim 2 is suggested or taught. So even with Bryers the references single or in combination do not suggest all the limitations in the claimed invention. Therefore, a Prima Facie case of obviousness has not been established and Claim 2 is patentable over the art of record.

Claim 22 depends on Claim 16. The limitations in Claim 16 are incorporated in Claim 22. As argued above and incorporated herein by reference, Claim 16, in part, calls for "extracting predefined parameters; using the predefined parameters to search a memory and identifying a cross reference index there from; using the cross reference

index associated with each received data packet to point to respective output register previously assigned to the corresponding flow of each receive data packet;" None of these elements is found in Salamat and/or Bryers, on which the Examiner relied in rejecting Claim 22. As argued above and incorporated herein by reference, the Examiner has not established a Prima Facie case of obviousness. Therefore, Claim 22 is patentable over the art of record.

Claim 12 (dependent on Claim 1) is rejected under 35 USC 103(a) as being unpatentable over Salamat, in view of Sasagawa as applied to claim 1 above ,and further in view of Yen(US20020150097A1). For this rejection the Examiner relied on Salamat and Yen.

Claim 12 depends on Claim 1 and all limitations of Claim 1 must be read into Claim 12. As a consequence, the limitations and arguments set forth above relative to Claim 1, as relate to Salamat, is equally applicable to Claim 12 and is incorporated herein by reference. Yen does not teach or suggest the limitations that applicants argued are not found in Salamat. Therefore, a Prima Facie case of obviousness has not been established relative to Claim12 and it is patentable over the art of record.

Regarding the rejection of Claim 12 as it depends on Claim 2, it is Applicants' contention the limitations and arguments set forth above relative to Claim 2 are equally applicable to Claim 12 and incorporated herein by reference. As a consequence, a Prima Facie case of obviousness has not been made and Claim 12, as it depends on Claim 2, is patentable over the art of record.

Claim 14 is rejected under 35 USC 103(a) as being unpatentable over Salamat, in view of Sasagawa as applied to Claim 1 above and further in view of Beshai (US20020083195A1).

Claims 14 depends on Claim 1. Therefore, all limitations of Claim 1 must be read into claim 14. As a consequence, the arguments and limitations set forth above in asserting that Claim1 is patentable over Salamat and Sasagawa are equally applicable

and incorporated herein by reference. Simply stated, the limitations, set forth above, found in Claim 1 are not found in the references. As a consequence, the Examiner has not established a Prima Facie case of obviousness and Claim 14 is patentable over the art of record.

Rejection of Claims 24-29

Claims 24 – 29 are rejected under 35USC 103(a) as being unpatentable over Salamat in view of Bryers. Bryers is cited for disclosing a CAM that ,according to the Examiner, could be used to modify Salamat with specific routing details to properly provide network services.

In response, applicants respectfully disagree with the Examiner and argue it would take much more than ordinary skill in the art to combine the CAM disclosed in Bryers with Salamat in order to render Claim 24 obvious. Even after the Examiner's combination the results would not teach or suggest all the elements of Applicants' Claim 24. In particular. Claim 24, in part, calls for "…providing a plurality of registers with each register associated with a flow; providing a cross reference table with each entry associated with a register within said plurality of registers;…..searching the cross reference table with parameters selected from the packets….." None of the recited steps are found in Salamat and/or Bryers , single or in combination. As argued above and incorporated herein by reference the Examiner is obliged to establish a Prima Facie case of obviousness. Failure to do so is evidence of non-obviousness. Therefore, Claim 24 is patentable over the art of record.

In Claim 24 each entry in the cross reference table is associated with a register within said plurality of registers. In contrast, Bryers [0550] states: "CAM 3144 maintains a list of pointers into FIFO 3144 for each of the data packets accepted by ring interface 3132. It is applicants' contention that the CAM in Bryers is used for a different purpose than what the cross reference table is used for in applicants Claim 24. As a consequence,

an artisan, without the aid of teachings from applicants' claim, would not used the CAM for a cross reference table as recited in Claim 24. Therefore, Claim 24 is patentable over the art of record.

In addition, applicants argue that the mapping of Claim 24 onto Salamat or visa versa is in error. Claim 24 calls for "providing a plurality of registers with each register associated with a flow". To find support in Salamat for this element, the Examiner states: "([0039] re-sequencing engine performs operations on distinct traffic streams)" Final Office Action, page 20.

Salamat [0039] states: "It should be understood that resequencing engine 82 can perform operations on, for example, 64 distinct traffic streams". It is applicants' contention that this statement is general and would not suggest "providing a plurality of registers with each register associated with a flow" as recited in Claim 24. As a consequence, Salamat alone or in combination with Bryers does not render Claim 24 obvious.

Claims 25, 26, and 27 depend on Claim 24. The limitations of Claim 24 are incorporated in the dependent Claims. As a consequence, Claims 25, 26, and 27 are patentable for the same reasons (identified above and incorporated herein by reference) that Claim 24 is patentable. With respect to Claim 25, Applicant is aware of the Examiner's position that Bryers, discloses the subject matter of Claim 25. Applicants have reviewed Bryers and could not find such teachings. Likwise, the Examiner contends the subject matter of Claims 26 and 27 are found in Salamat. The Examiner relied on [0012] Salamat to support his position. A review of Salamat did not find any teachings that could reasonably be construed to disclose or suggest the subject matter of Claims 26 or 27.

Claims 28 and 29, due to its dependency on Claim 28, calls for ,in part, "…a second instruction module with instructions that use the predetermined extracted predefined parameters to search an index table having multiple entries with each of

said multiple entries associated with a different register…" Neither Salamat single or in combination with Bryers disclose or suggest this limitation. Therefore, the Examiner has not established a Prima Facie case of obviousness. As argued above and incorporated herein by reference, failure to do so is evidence of non obviousness. Therefore, Claims 28 and 29 are patentable over the art of record.

The mapping of the above limitation of Claim 28, at pages 22 and 23 of the Office Action, to Salamat and/or Bryers by the Examiner is some what confusing. It appears the Examiner is relying on paragraphs [0010], [0028] of Salamat, and [0550] of Bryers for teaching this limitation. It is applicants' contention that this reliance is misplaced and in error. Paragraph [0010] of Salamat relates to reduced storage for storing sequence numbers of packets and paragraph [0028] refers to sequence space in the form of memory 94. Likewise, [0550] of Bryers refers to a cam. None of the references relied on by the Examiner suggest 'searching an index table having a plurality of entries with each entry associated with a different register'. Because the references mention memory and CAM which are in no way associated with registers as set forth in the Claim should not be sufficient to render the Claim obvious. As a consequence, this limitation is not found or suggested in the references and Claims 28 and 29 are patentable over the art of record.

In addition Claim 29 is patentable distinct for what it recites. The Examiner relied on paragraph [0550] of Bryers for teaching this element. It is applicants' contention Bryers is using the CAM for a different purpose than what is recited in Claim 29. As a consequence a prima facie case of obviousness has not been established and Claim 29 is patentable over the art of record.

Claim 30 is rejected under 35 USC 103(a) as being unpatentable over Salamat, in view of Bryers, and further in view of Beshai. The Examiner states: "Bryers discloses a cross reference index table ([0550] content addressable memory)". The Examiner relied

on Beshai for disclosing "a plurality of switching planes ; a buffer for storing packets transported through said switching planes.

It is Applicants' contention that the Examiner has not established a prima facie case of obviousness relative to Claim 30. As argued above and incorporated herein by reference, a prima facie case of obviousness is established if all the limitations of Claim 30 are found in the cited references single or in combination. The references do not disclose or suggest the following limitations:"…a register stack wherein each register is associated with a different flow of a multi flow system; a cross reference index table having a plurality of entries with each entry associated with a different register in said register stack" As a consequence, a Prima Facie case of obviousness has not been made and Claim 30 is patentable over the art of record.

Applicants have reviewed the Examiner's argument and respectfully disagree. Applicants contend the references, singly or in combination, do not disclose or suggest the relationship between registers in the register stack and flows in the multi flow system and/or the relationship between entries of the cross reference table and registers of the register stack. As argued above and incorporated herein by reference the Examiner's reliance on Bryers for teaching " a cross reference index table having a plurality of entries with each entry associated with a different register in said register stack;" is in error. The disclosure of a CAM in Bryers is insufficient to suggest this element of Claim 30 to an artisan. Likewise , as argued above and incorporated herein by reference, reliance on Salamat for suggesting or teaching "a system for ensuring packets are in predefined sequence……including a register stack wherein each register is associated with a different flow of a multi flow system is insufficient. The teaching of "sequence space in the form of memory 94" is insufficient to suggest or teach this element of applicants' claim to someone of ordinary skill in the art. As a consequence, even after the Examiner's combination the resulting structure would not render Claim 30 obvious.

Allowable Subject Matter

Claims 10, 15, and 21 would be allowed if re written in independent form including all limitations in the base claim and any intervening claims. These claims have been re written in independent form and are now in condition for allowance which is respectfully requested.

CONCLUSION

It is believed the present amendment answers all issues raised in the subject Office Action . Reconsideration is hereby requested and an early allowance of Claims 1-30 is solicited.

After review of this application if the Examiner still believes that the rejected Claims are not patentable over the art of record, Applicants respectfully request that this version of the Claims be entered for purpose of appeal.

Respectfully Submitted,

Dated: February 16, 2010

/Joscelyn G Cockburn/

Joscelyn G Cockburn
Attorney for Applicants
Reg. # 27069
Customer # 25299
(919) 876 7721